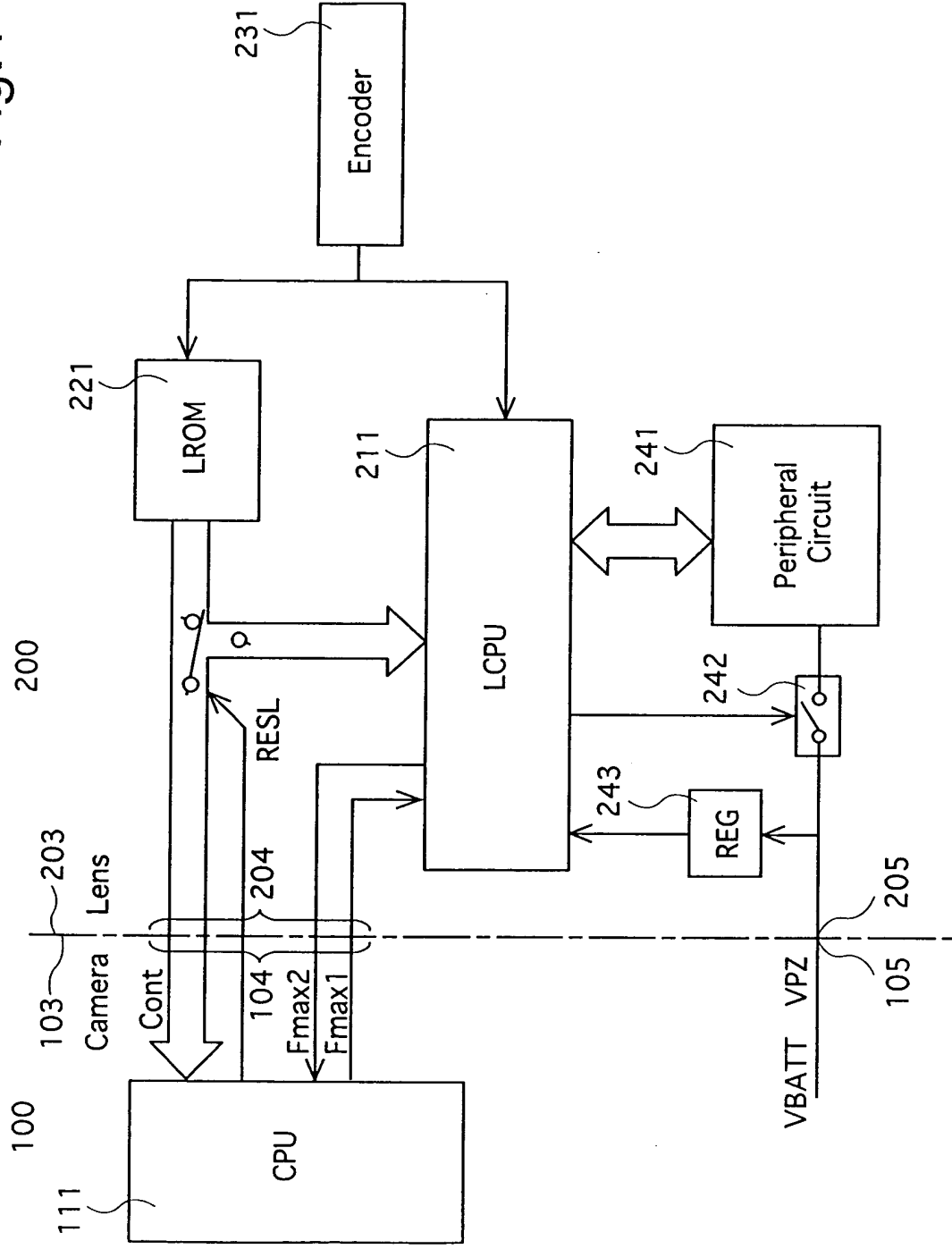


Fig.1



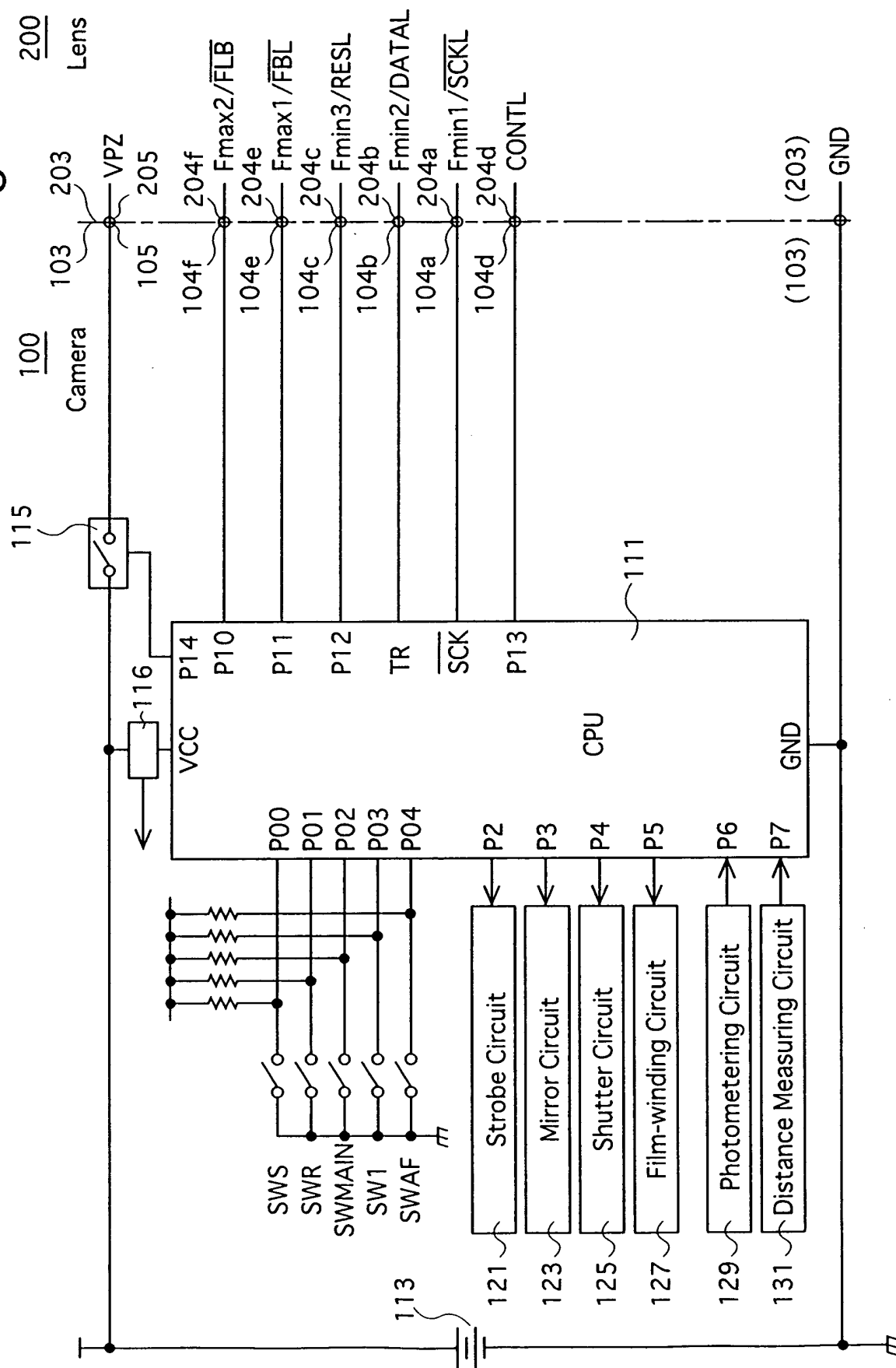
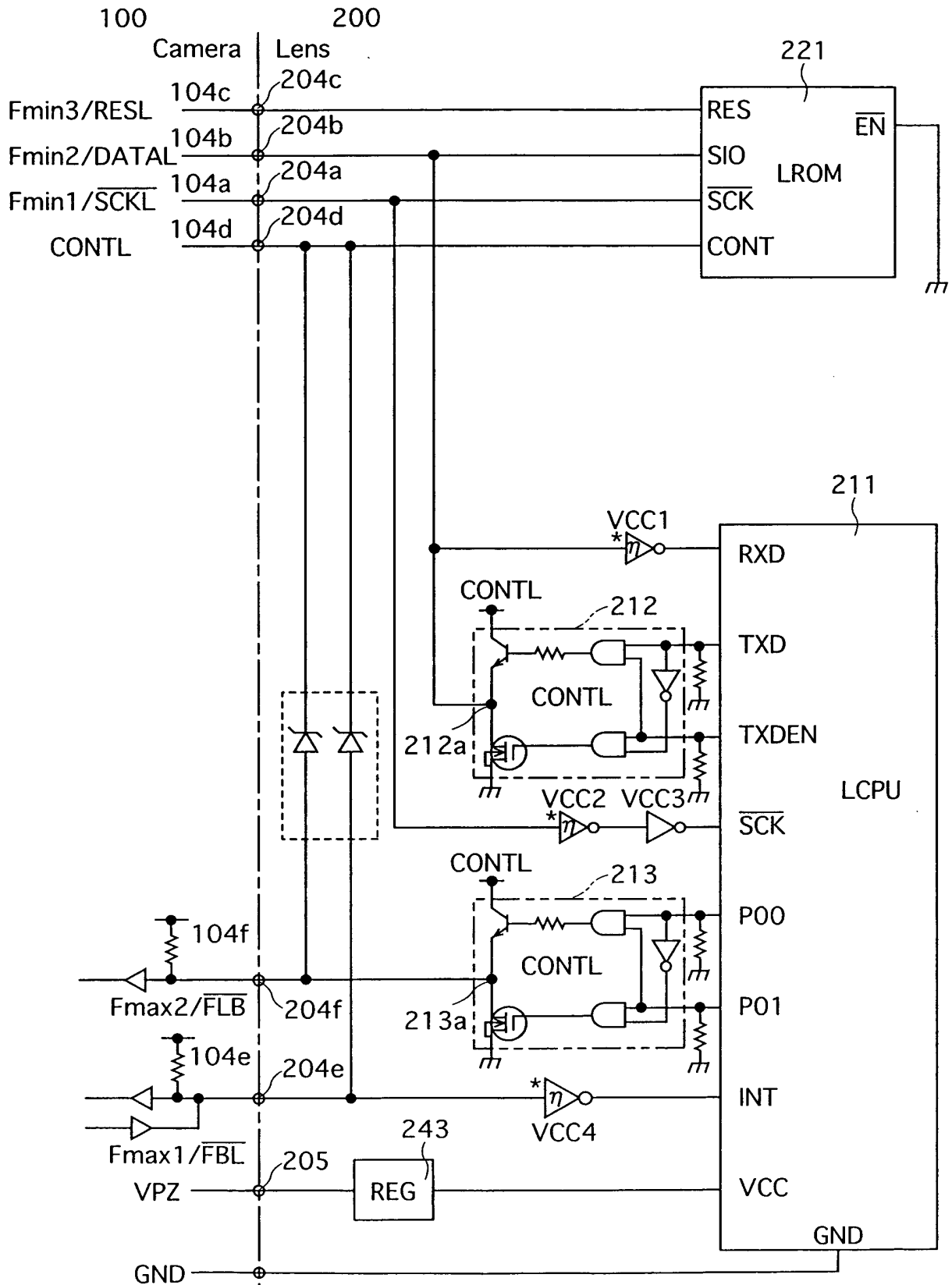


Fig.3



10083619.022702

Fig.4

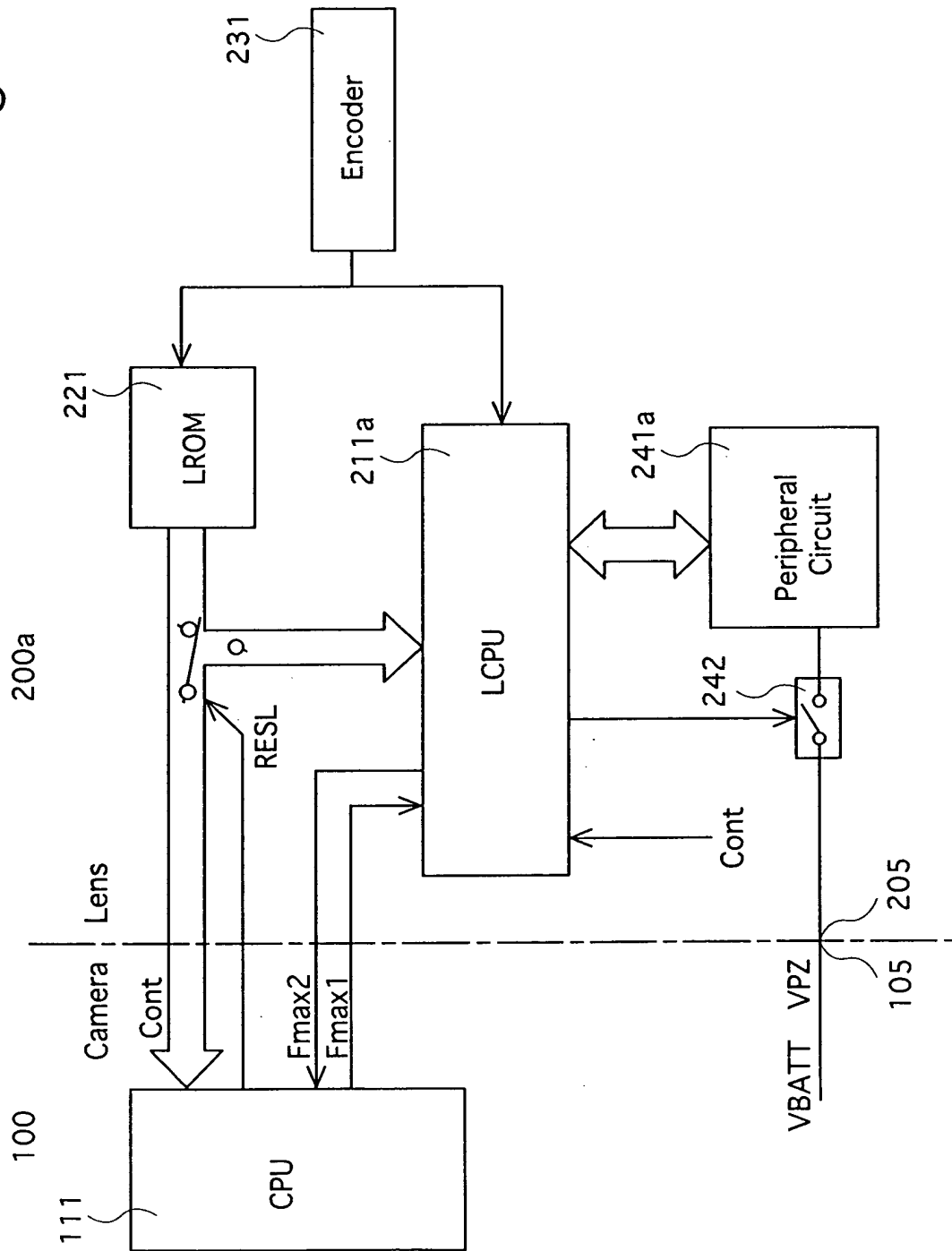


Fig.5

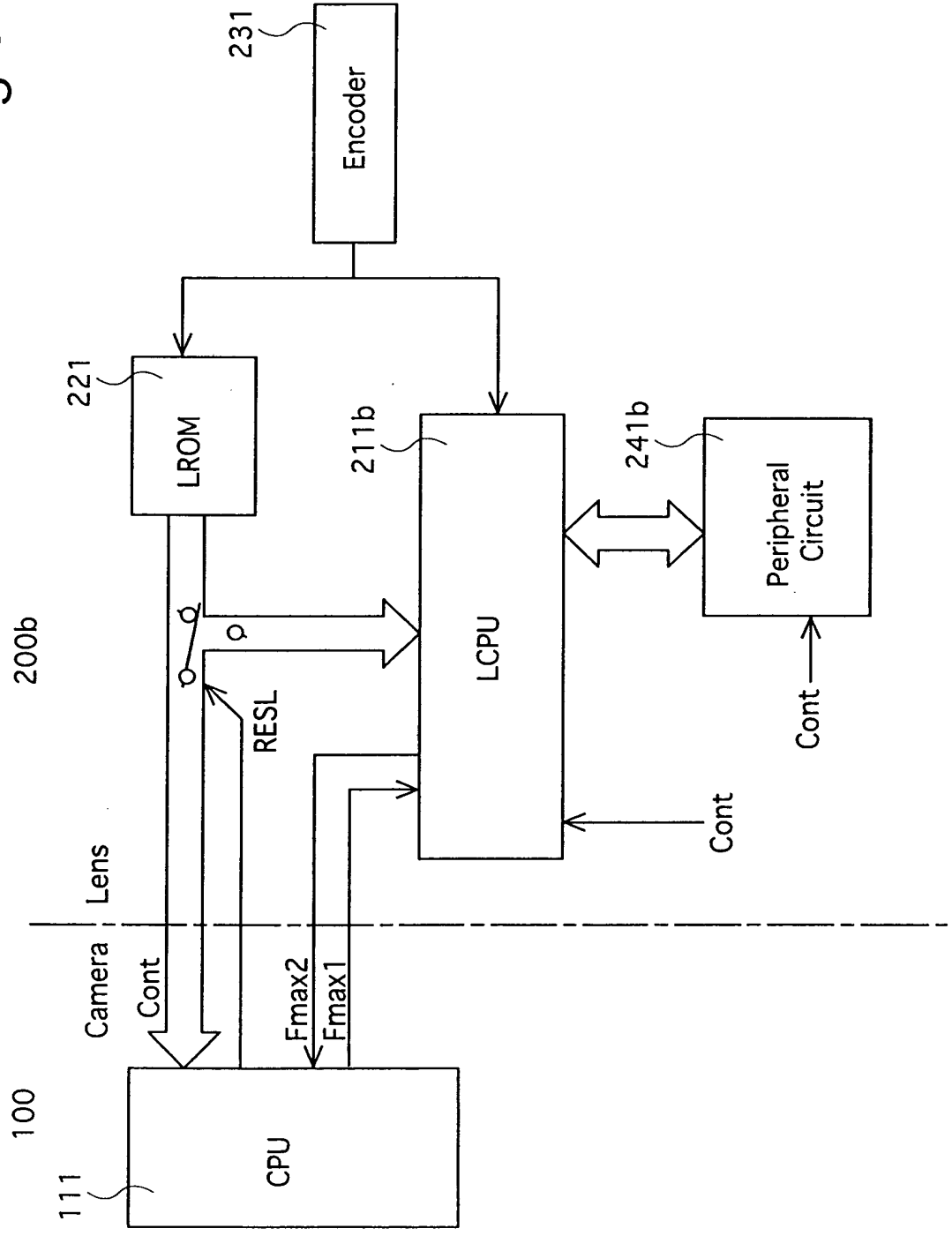
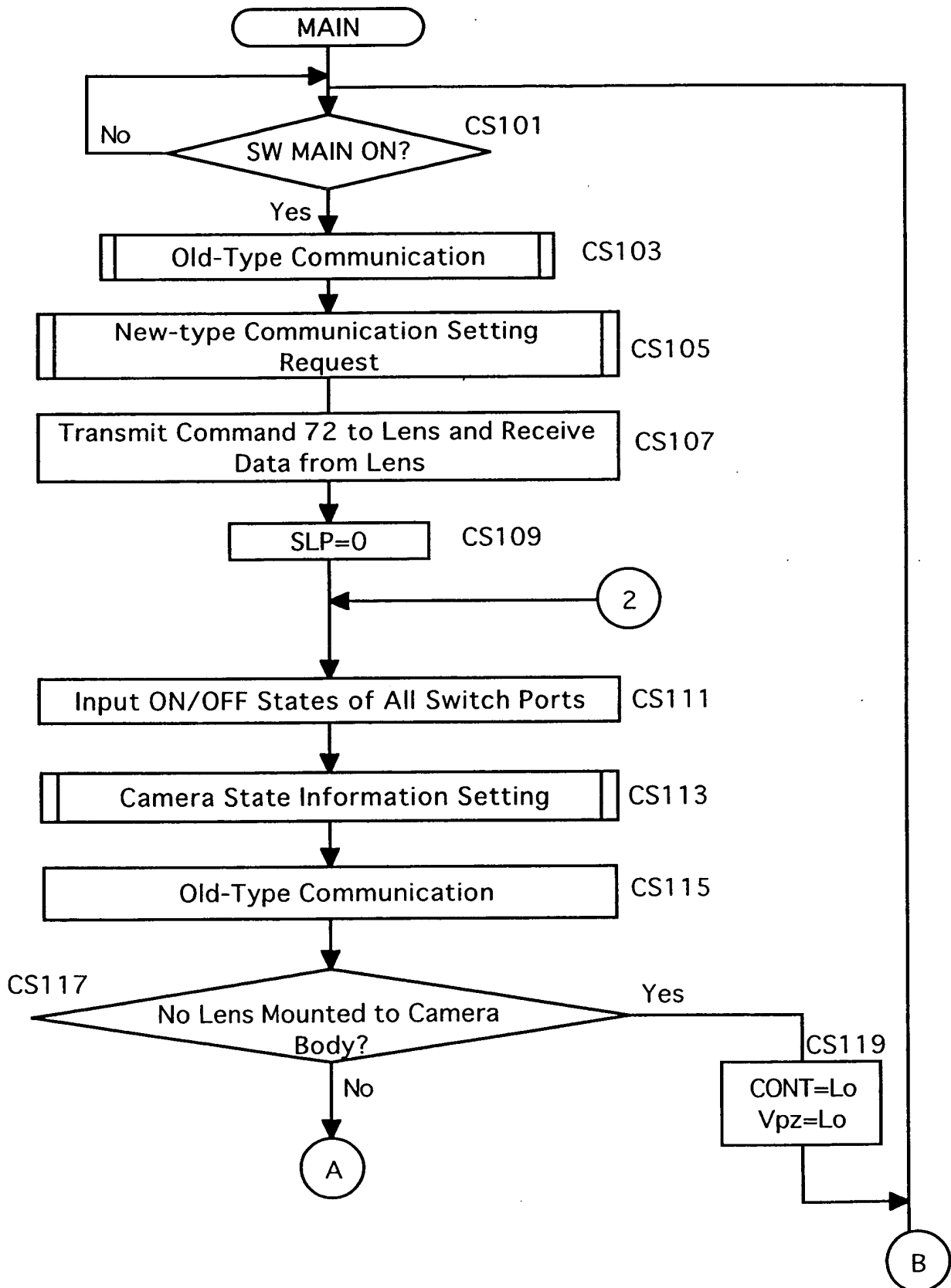


Fig. 6A



10083619.022702

Fig. 6B

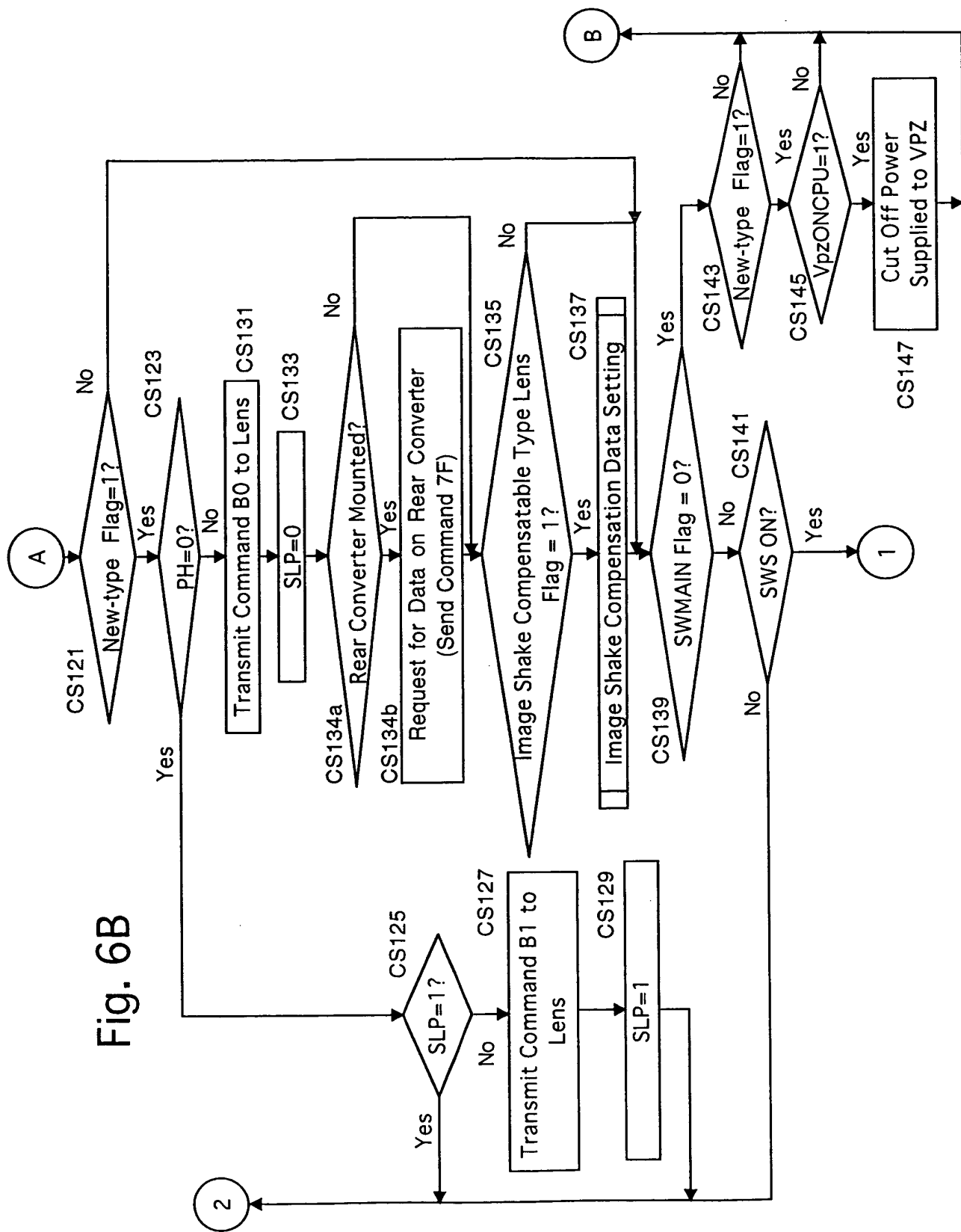
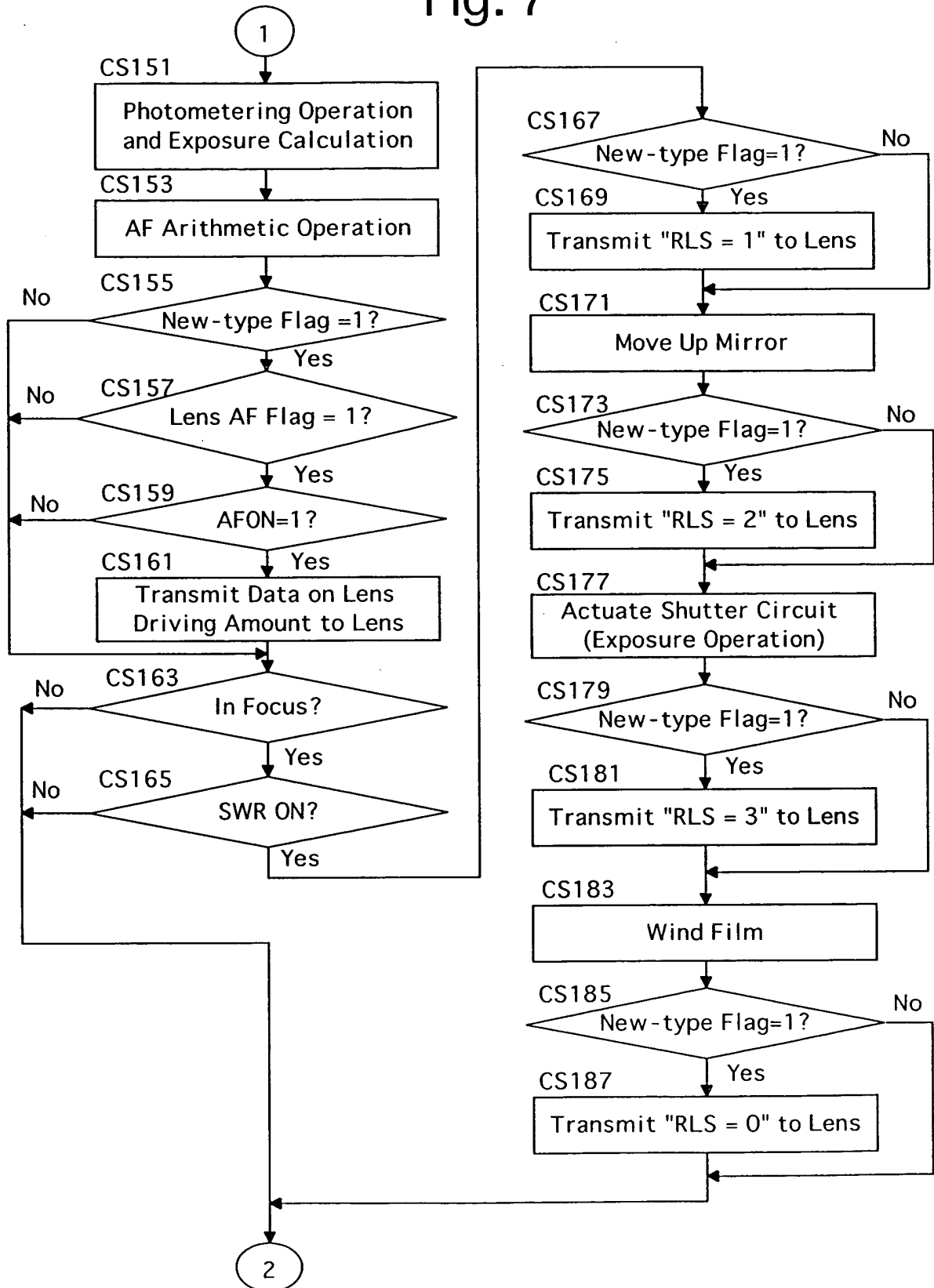


Fig. 7



10083619.022702

Fig. 8A

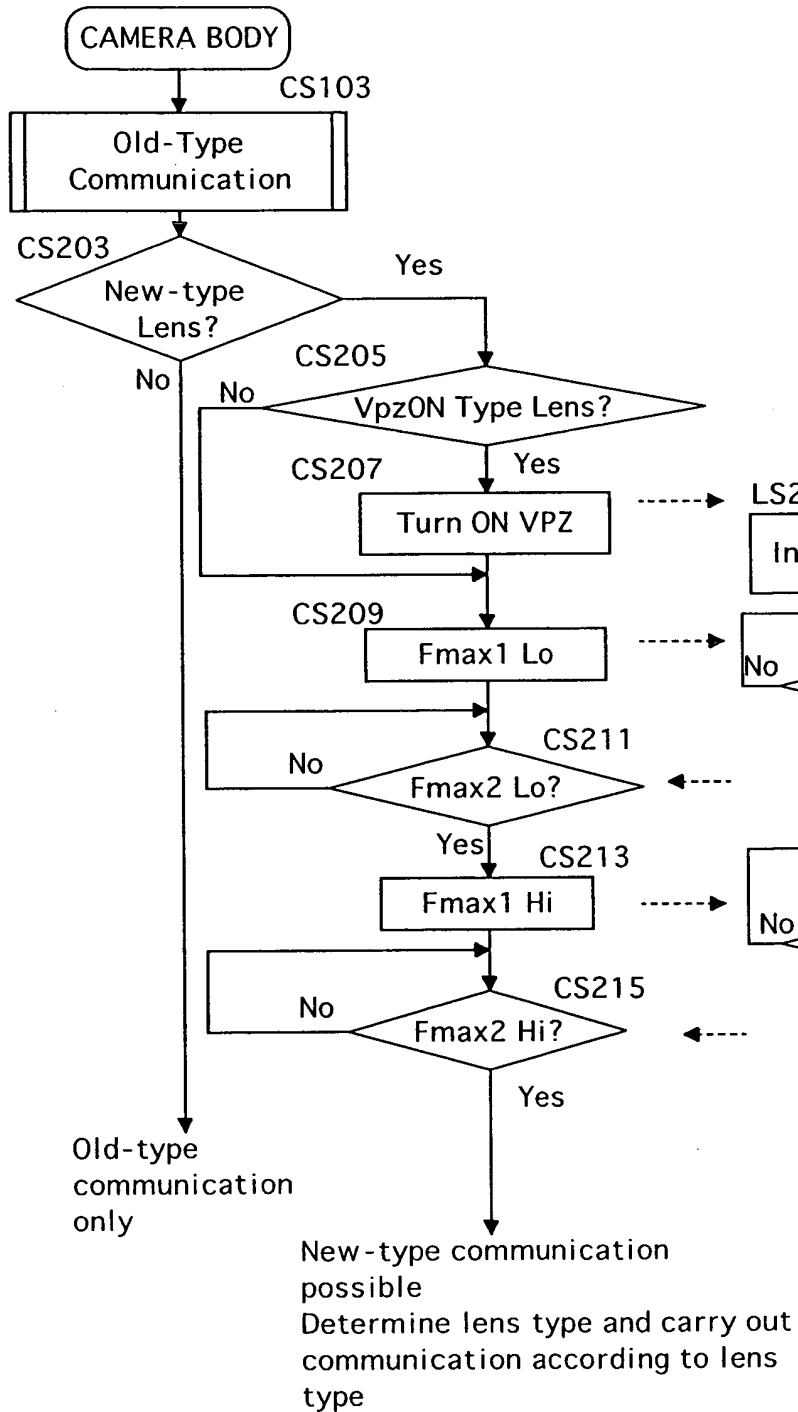


Fig.8B

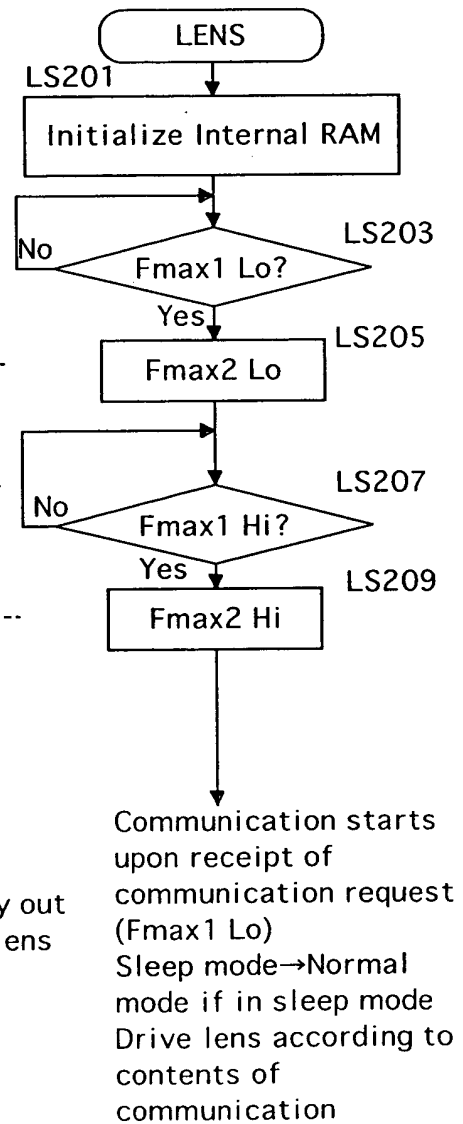
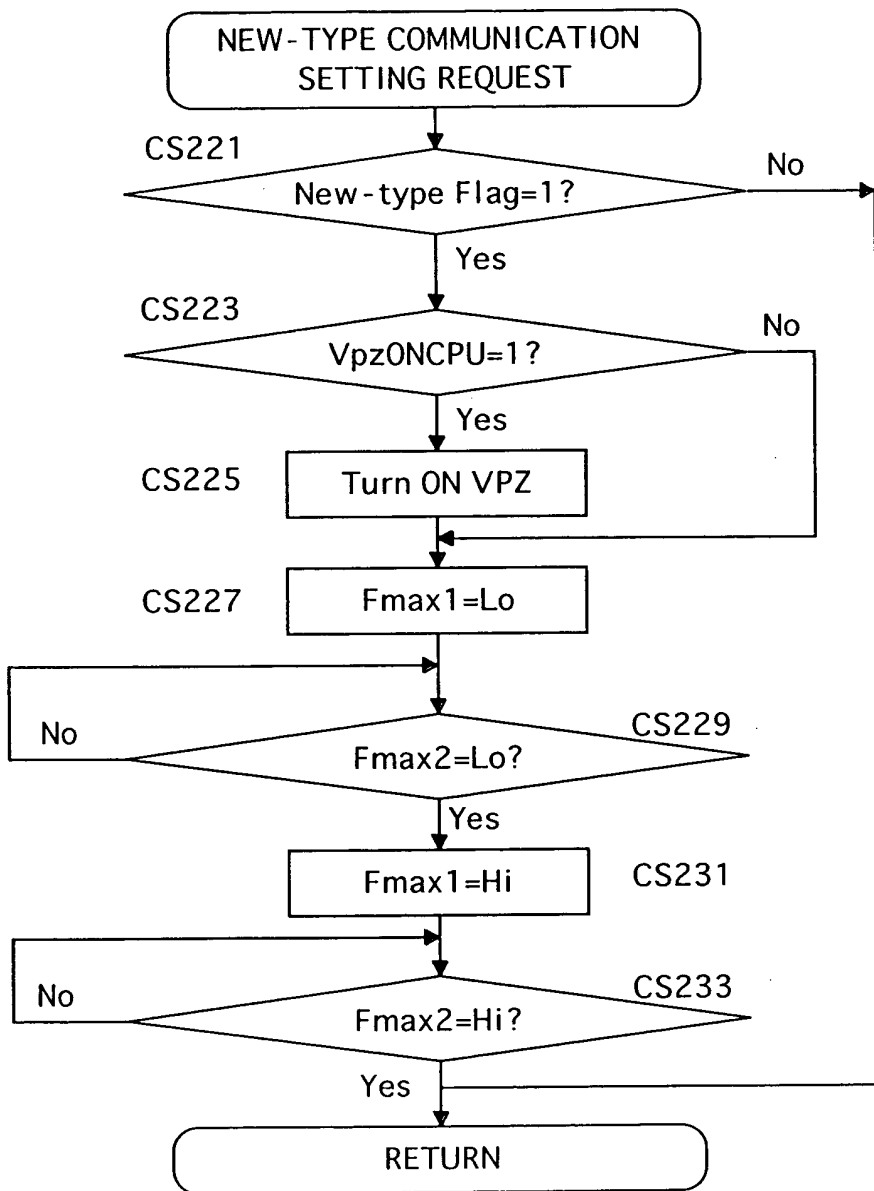
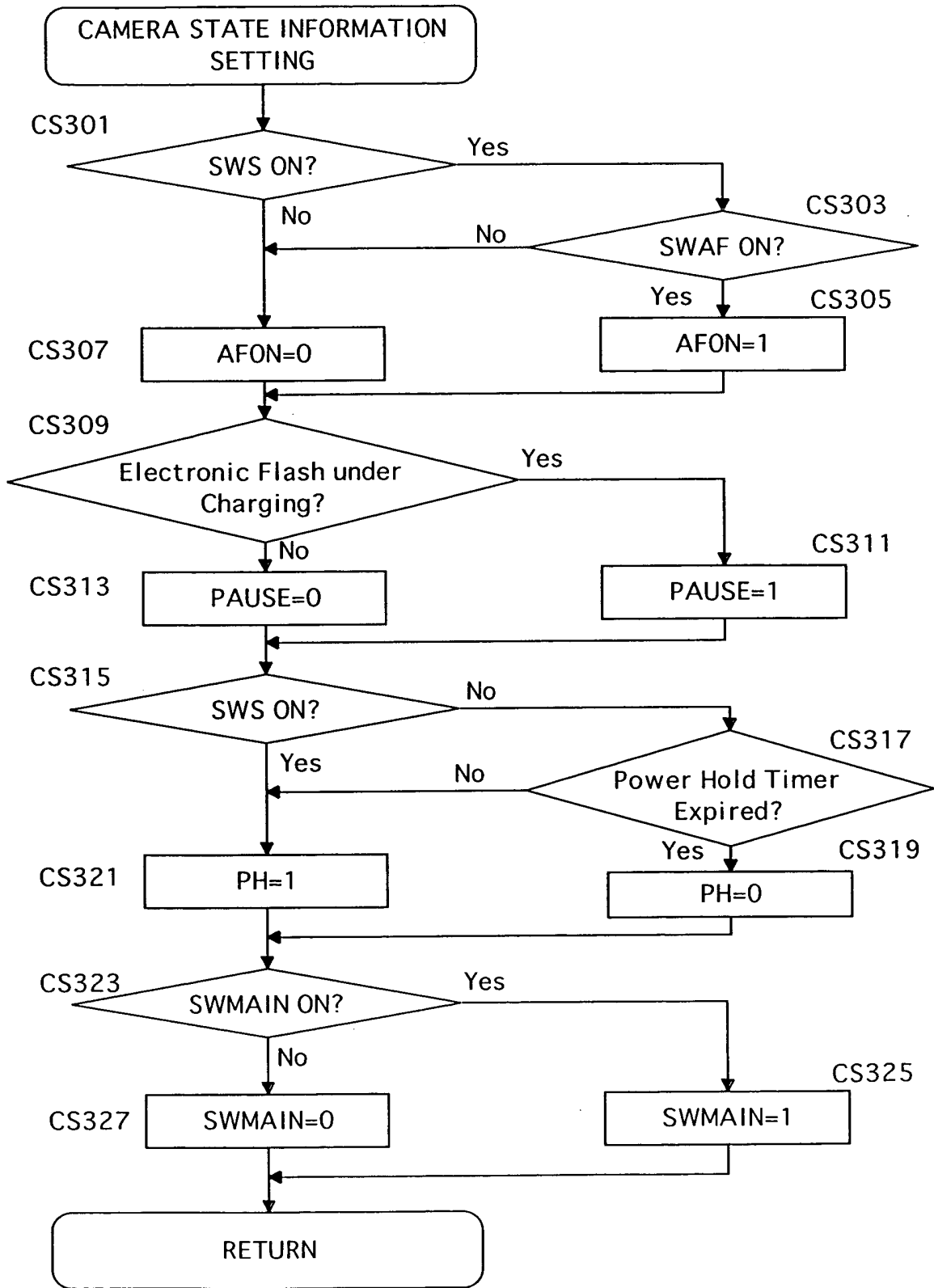


Fig.9



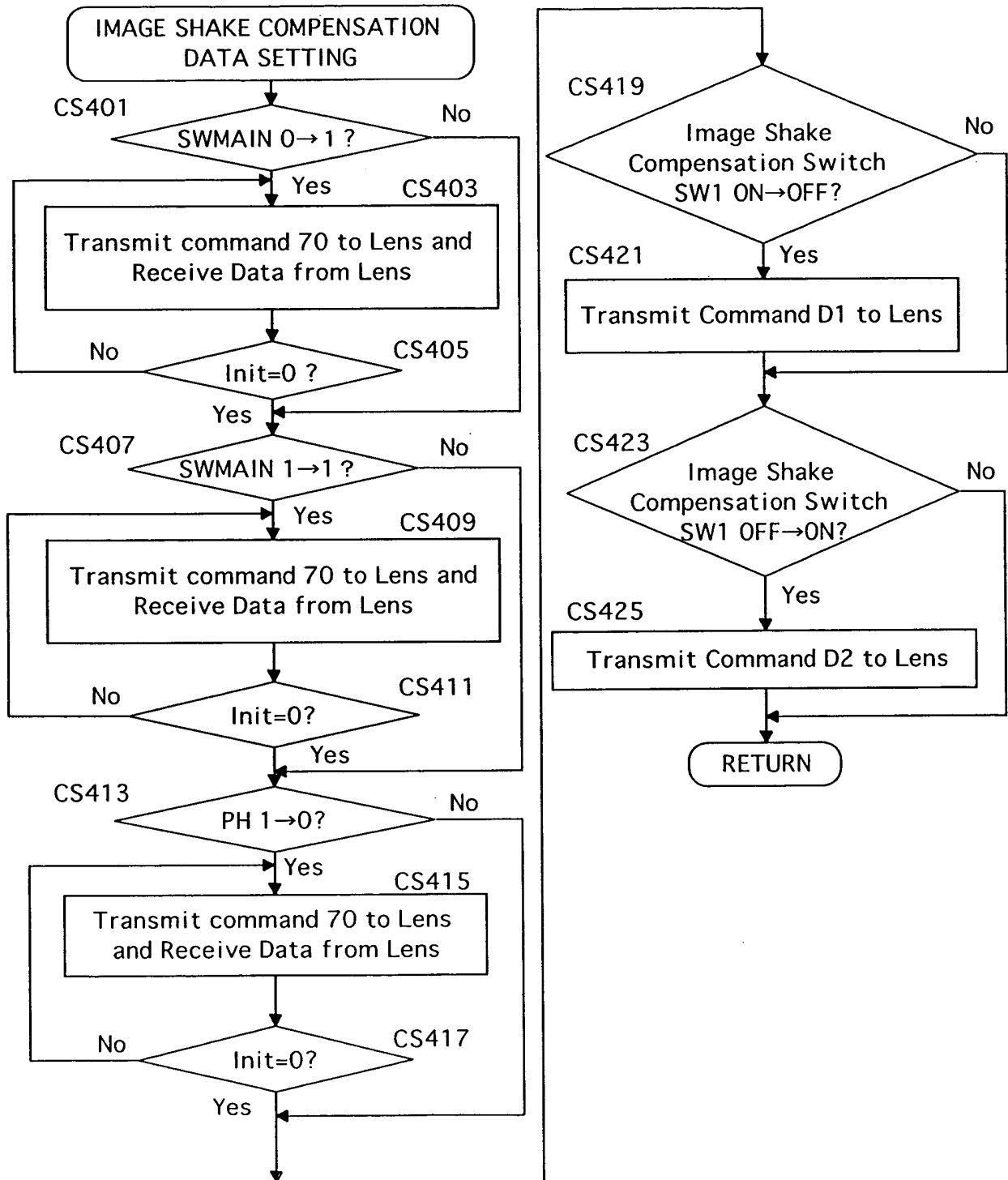
10083519.022702

Fig.10



10083619.022702

Fig.11



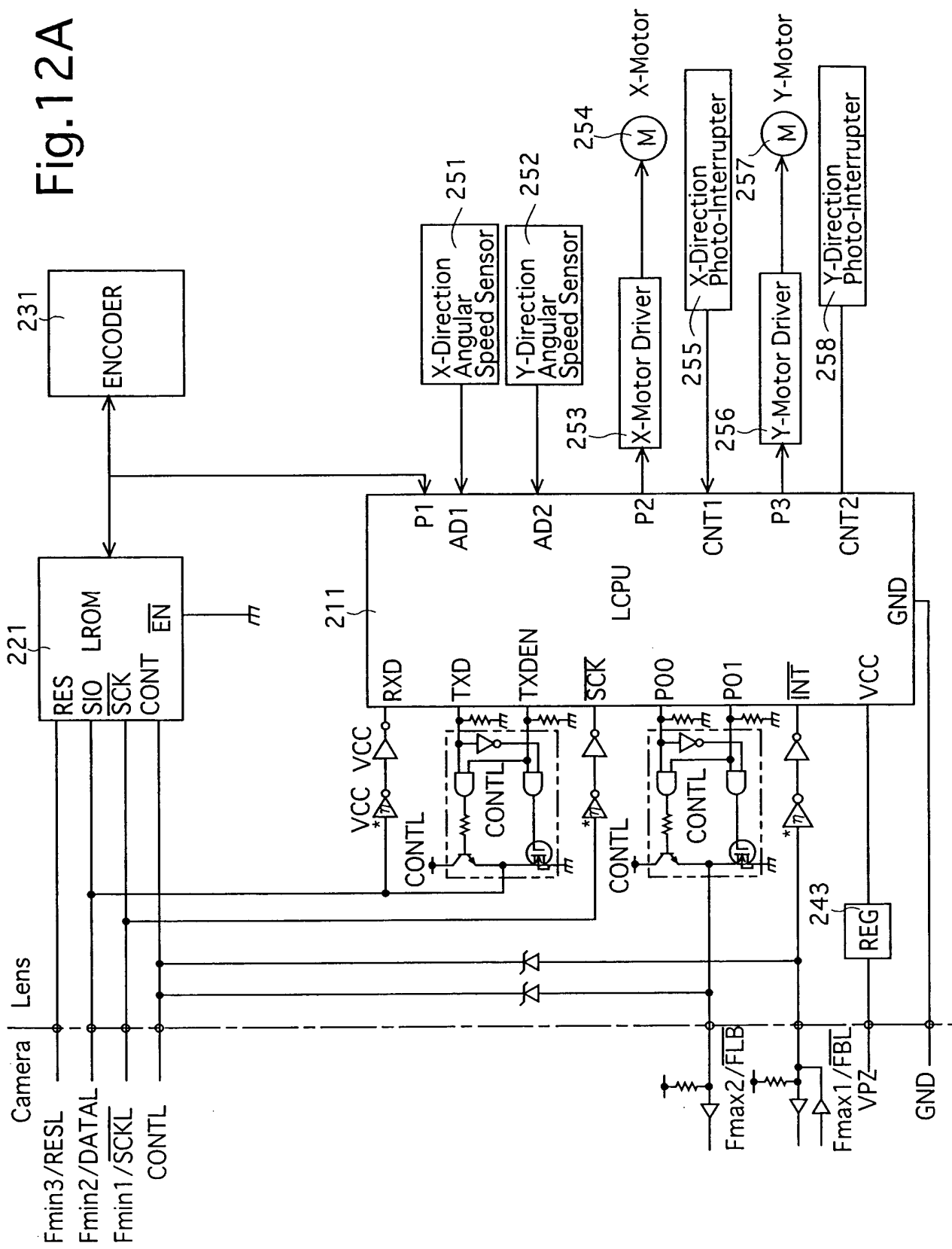


Fig.12A

Fig. 12B

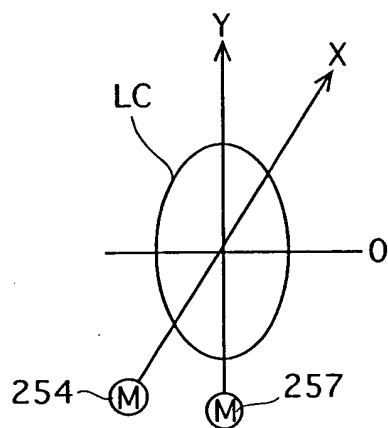
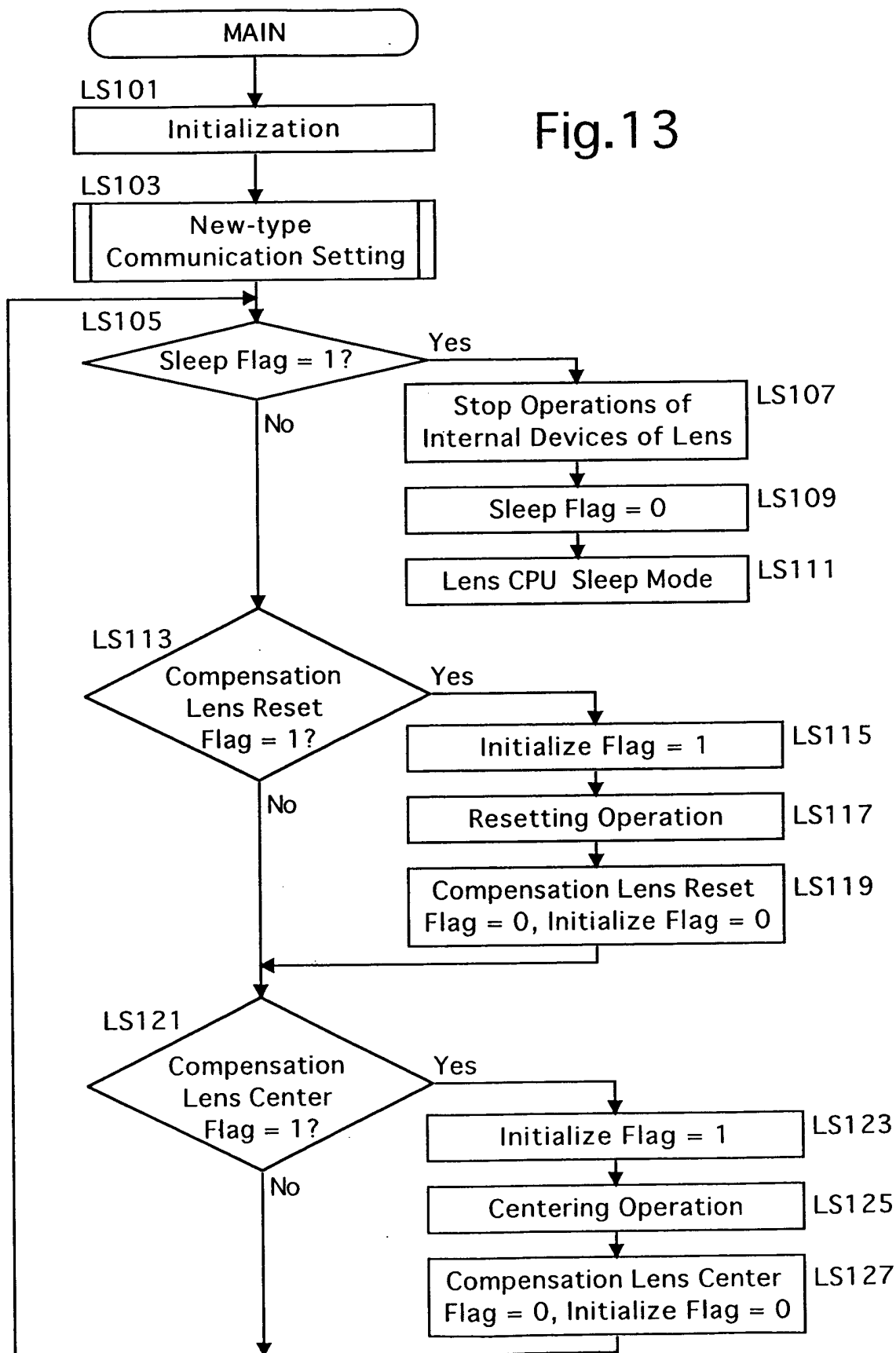
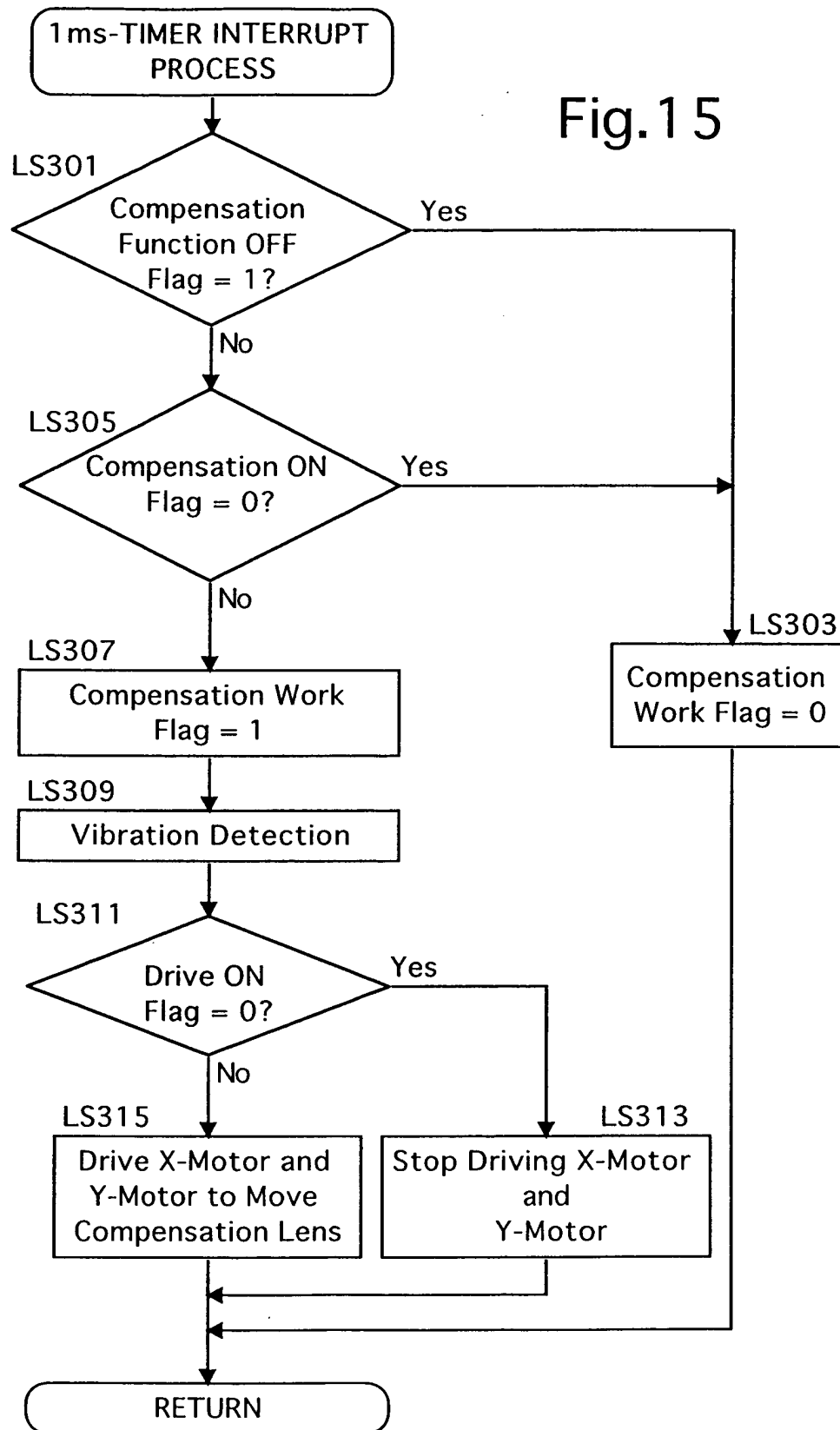


Fig.13



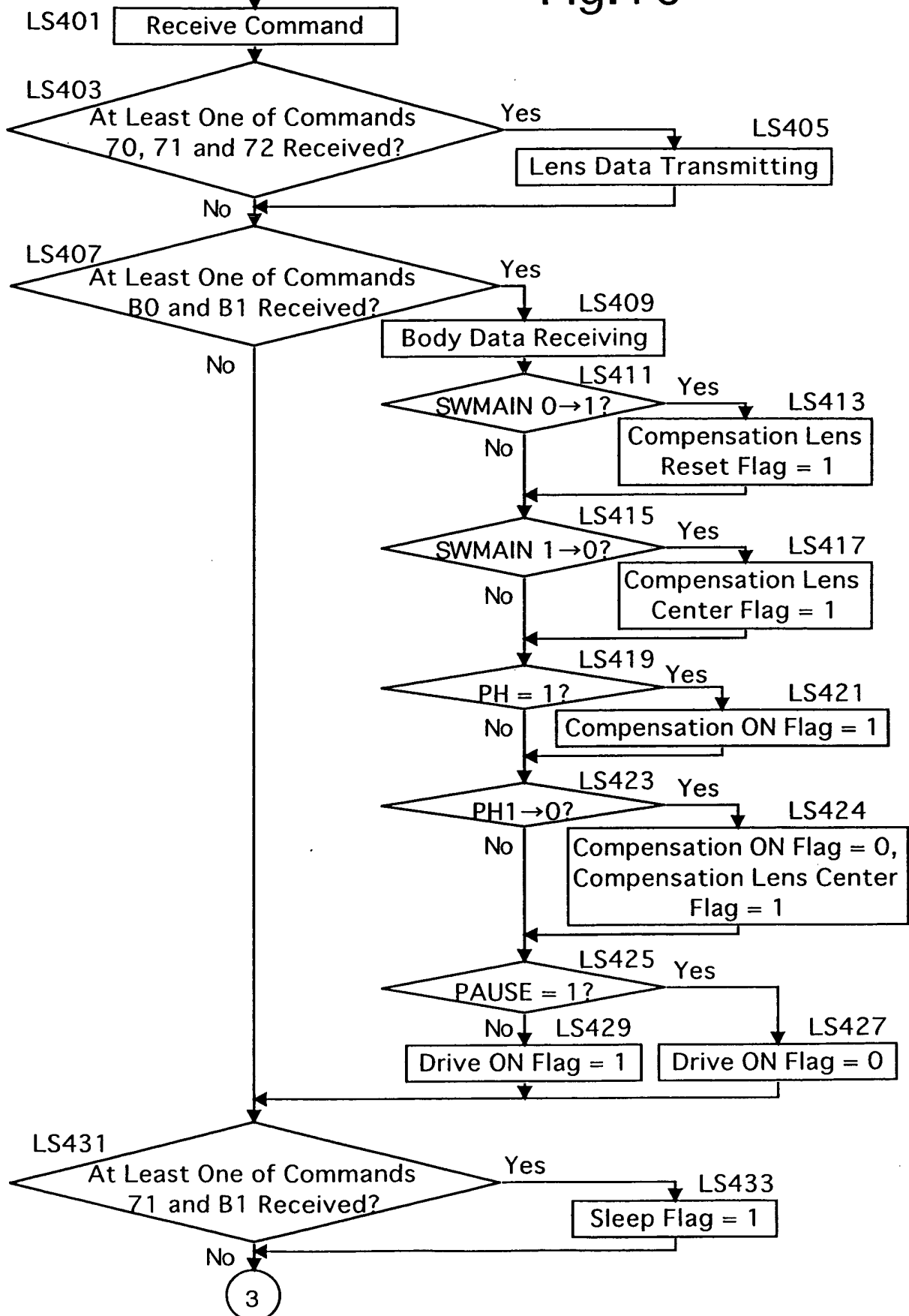
10083619-022702

Fig.15



INVERSE-INT INTERRUPT PROCESS

Fig.16



10083619.000702

Fig.17

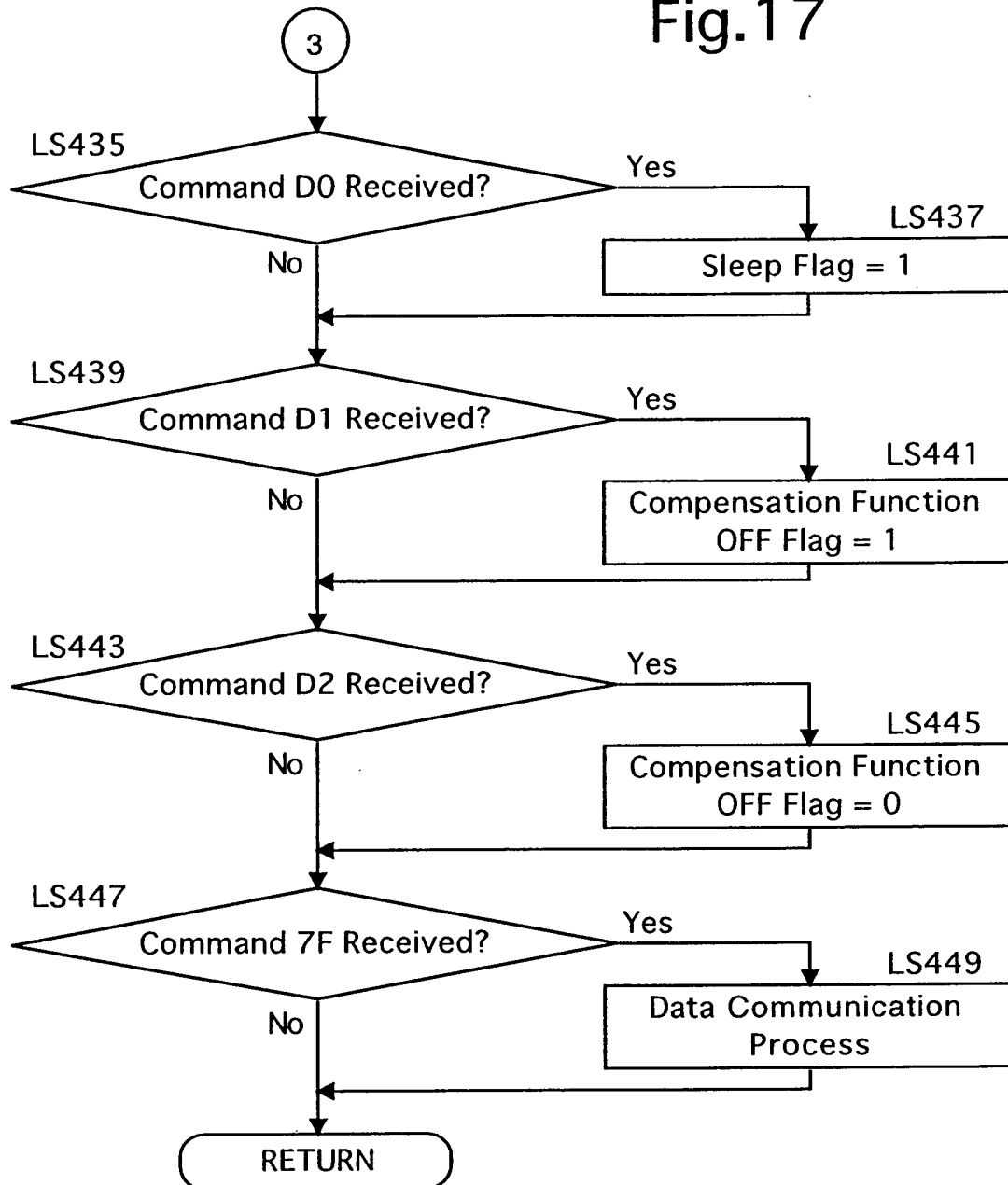


Fig. 18

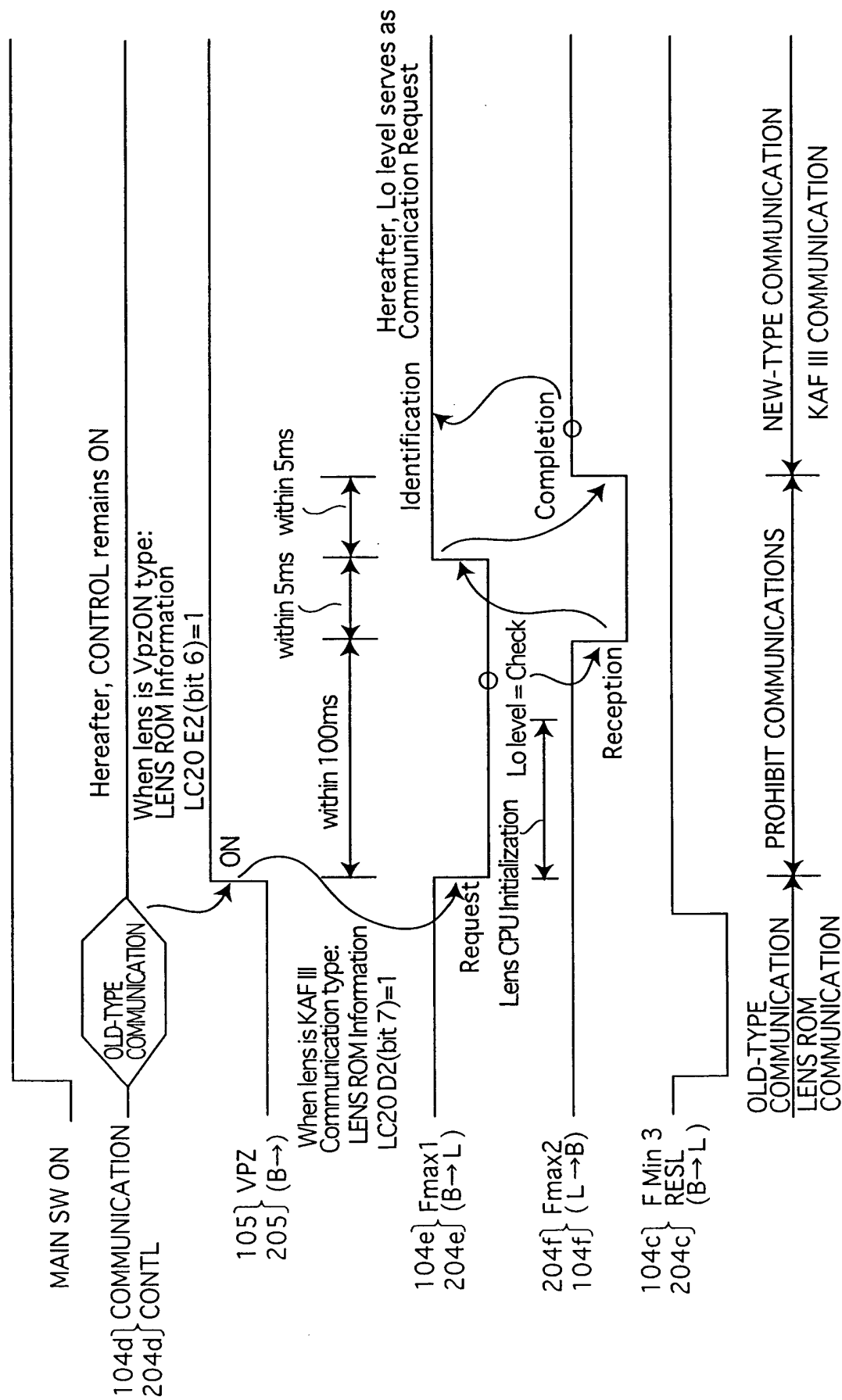


Fig. 19A

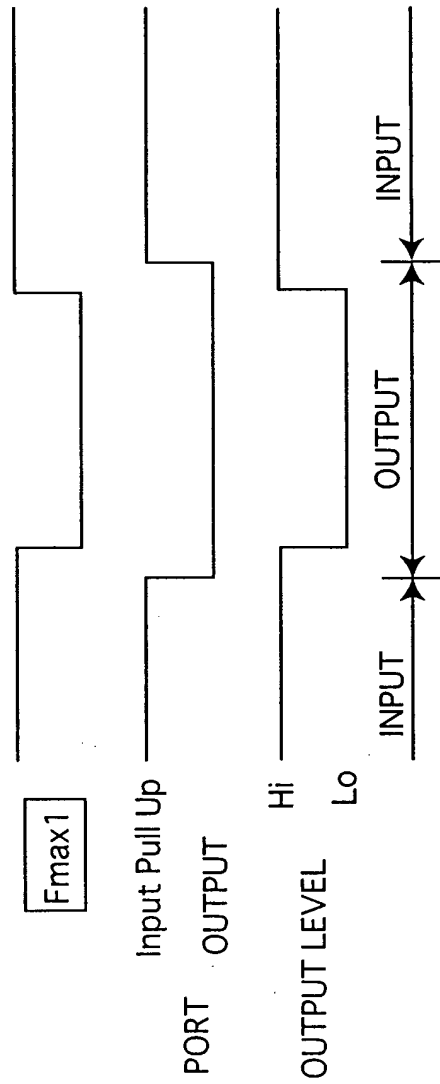


Fig. 19B

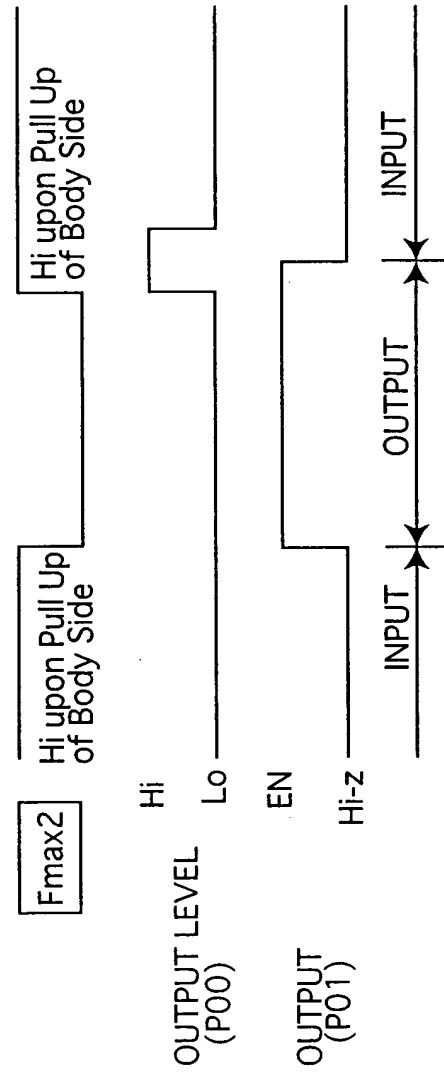


Fig. 20

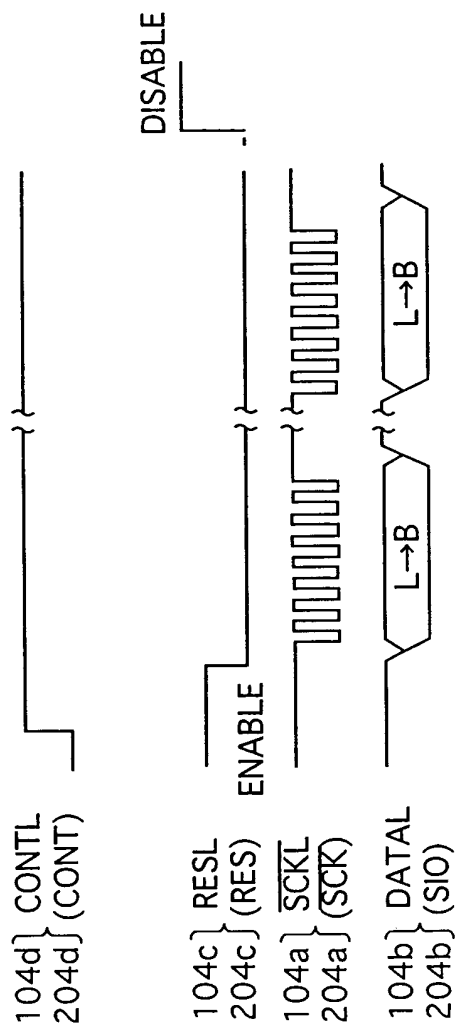
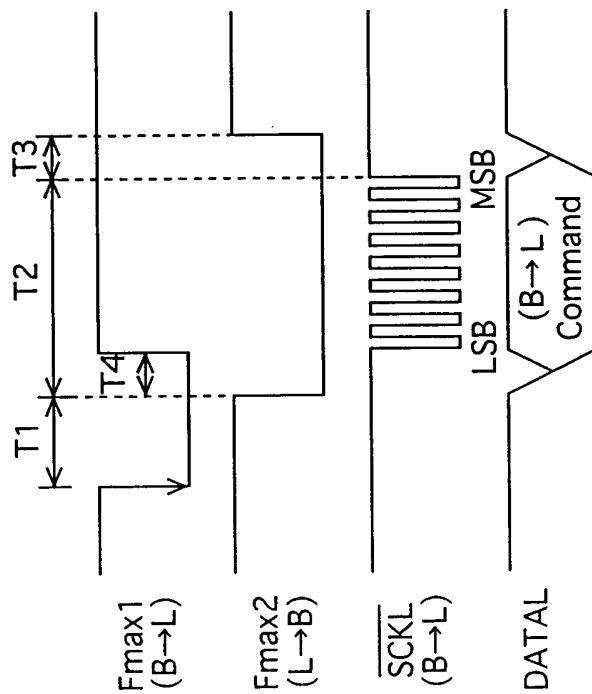


Fig.21A



- T1: within 50ms
- T2: within 5ms
- T3: within 5ms
- T4: within 5ms
- T5: within 5ms
- T6: within 5ms
- T7: within 5ms
- T8: within 5ms
- T9: within 5ms

Fig.21B

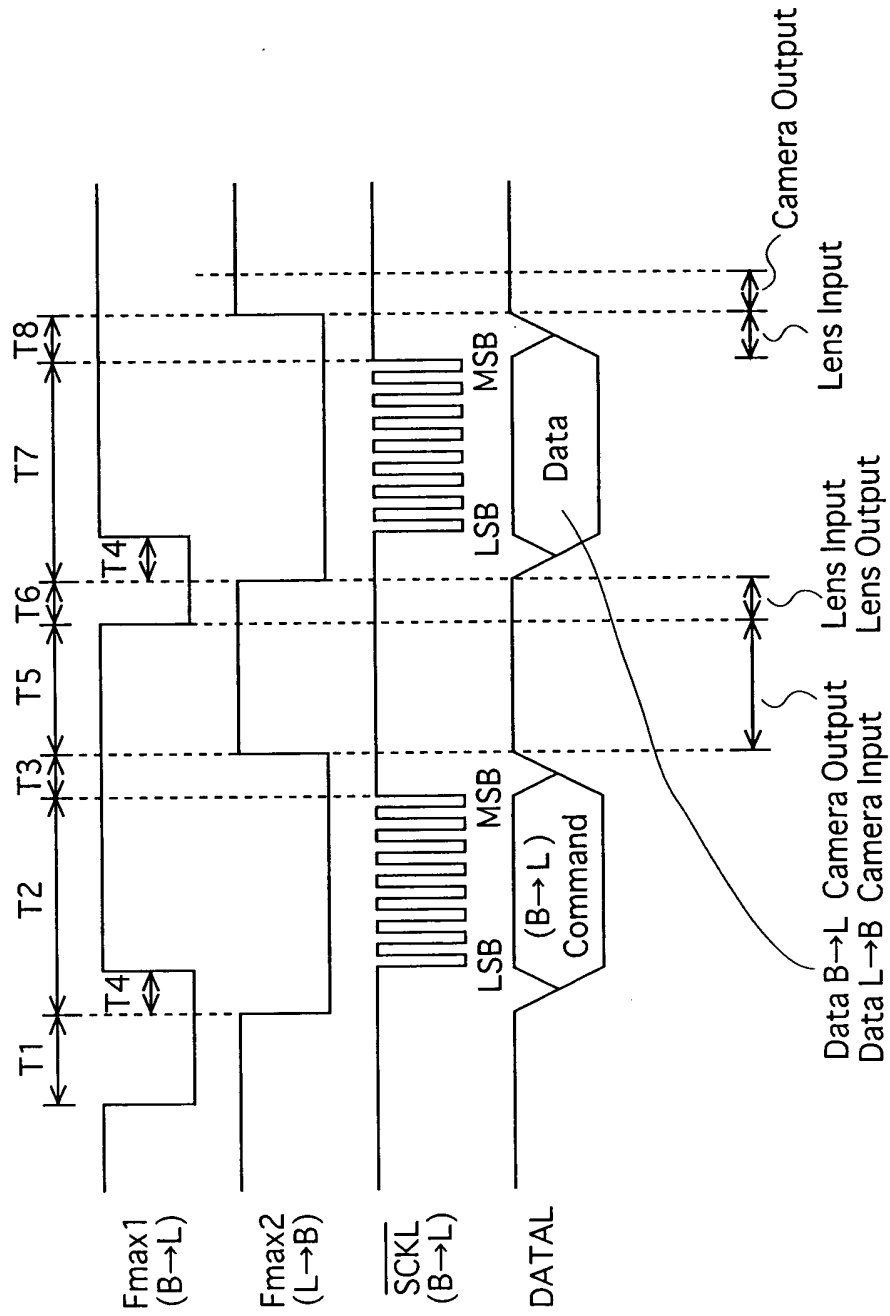
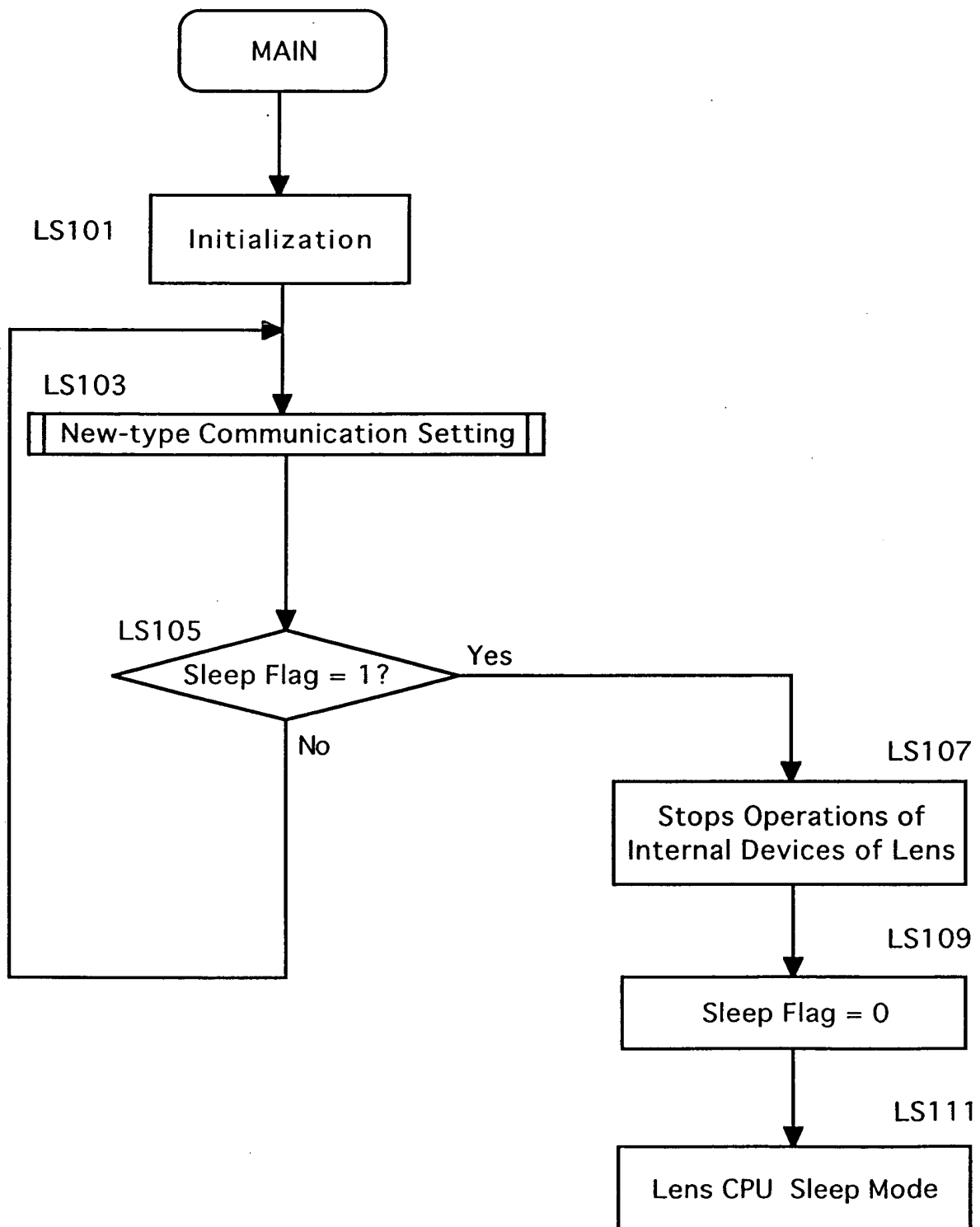
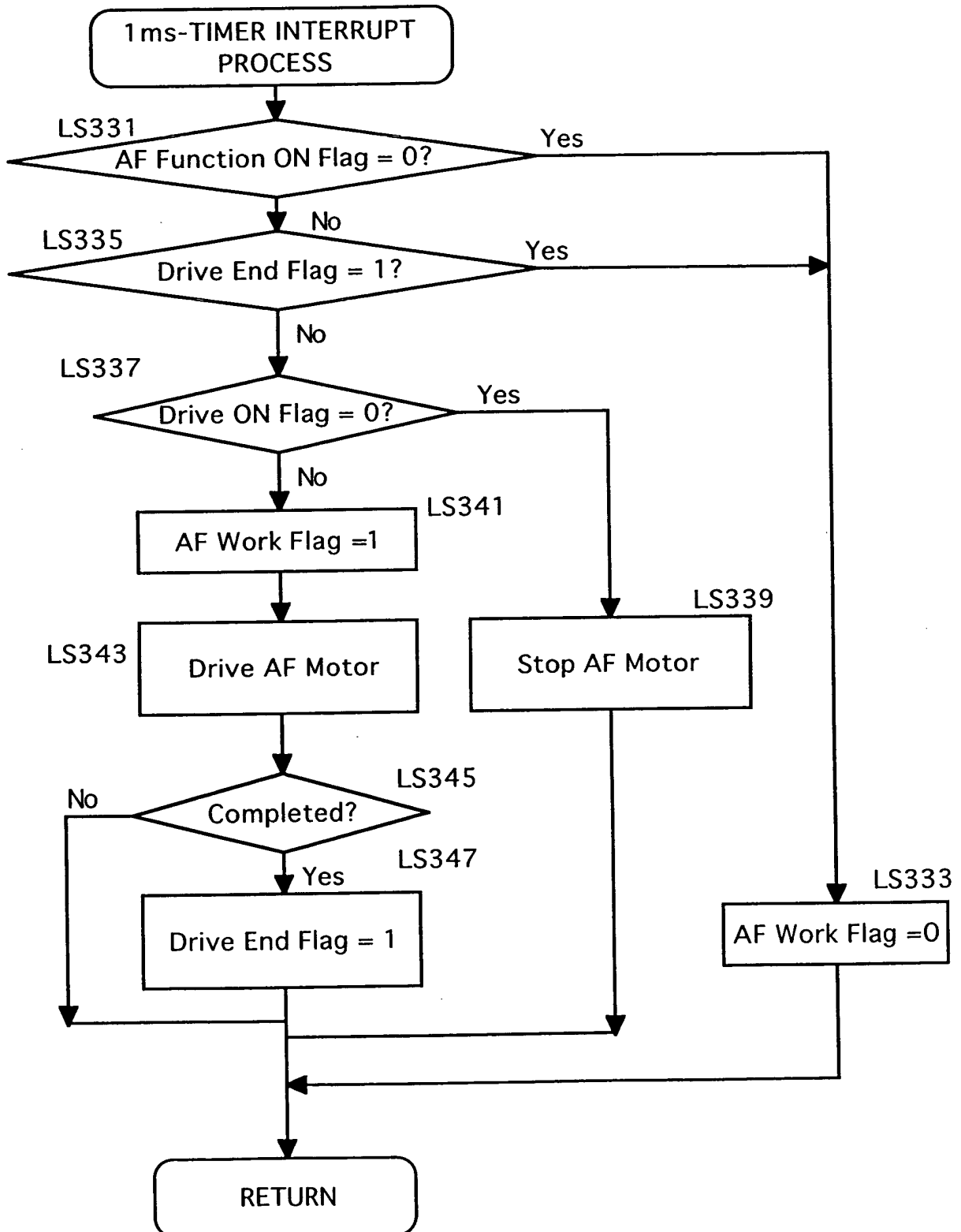


Fig. 23



10003619.022702

Fig. 24



10083619.022702

INVERSE INT INTERRUPT PROCESS

Fig. 25

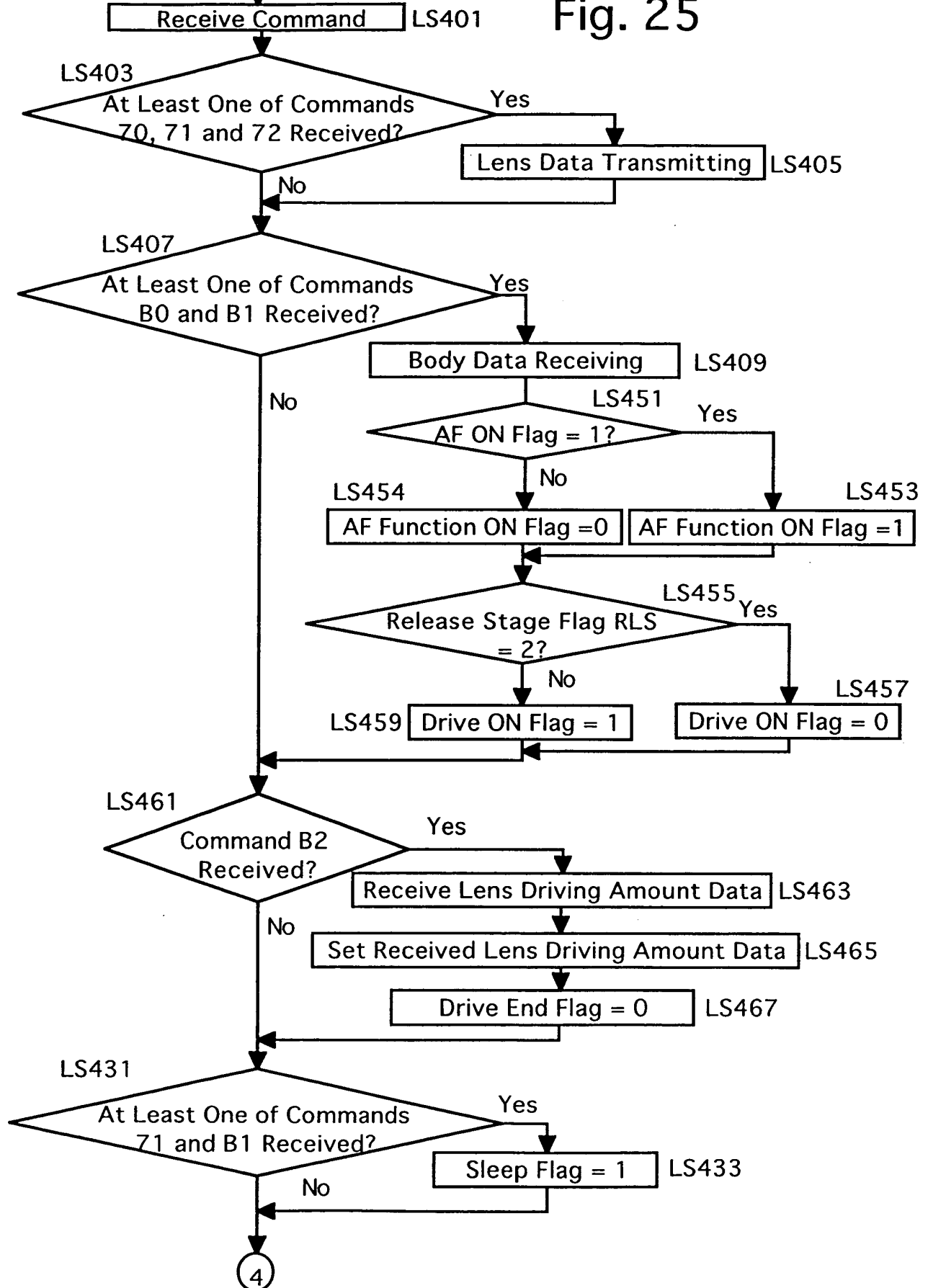
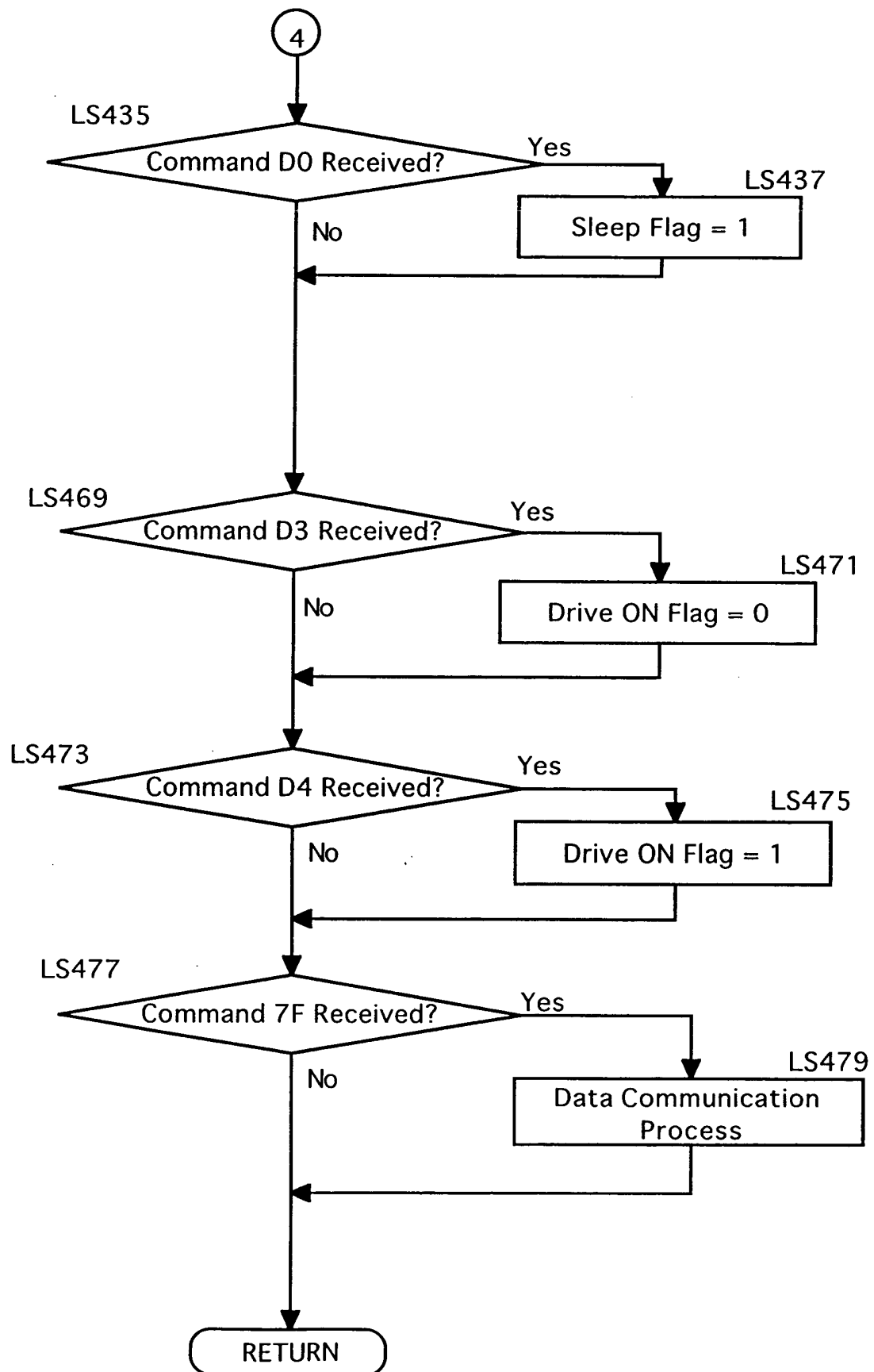


Fig. 26



10033619 032702